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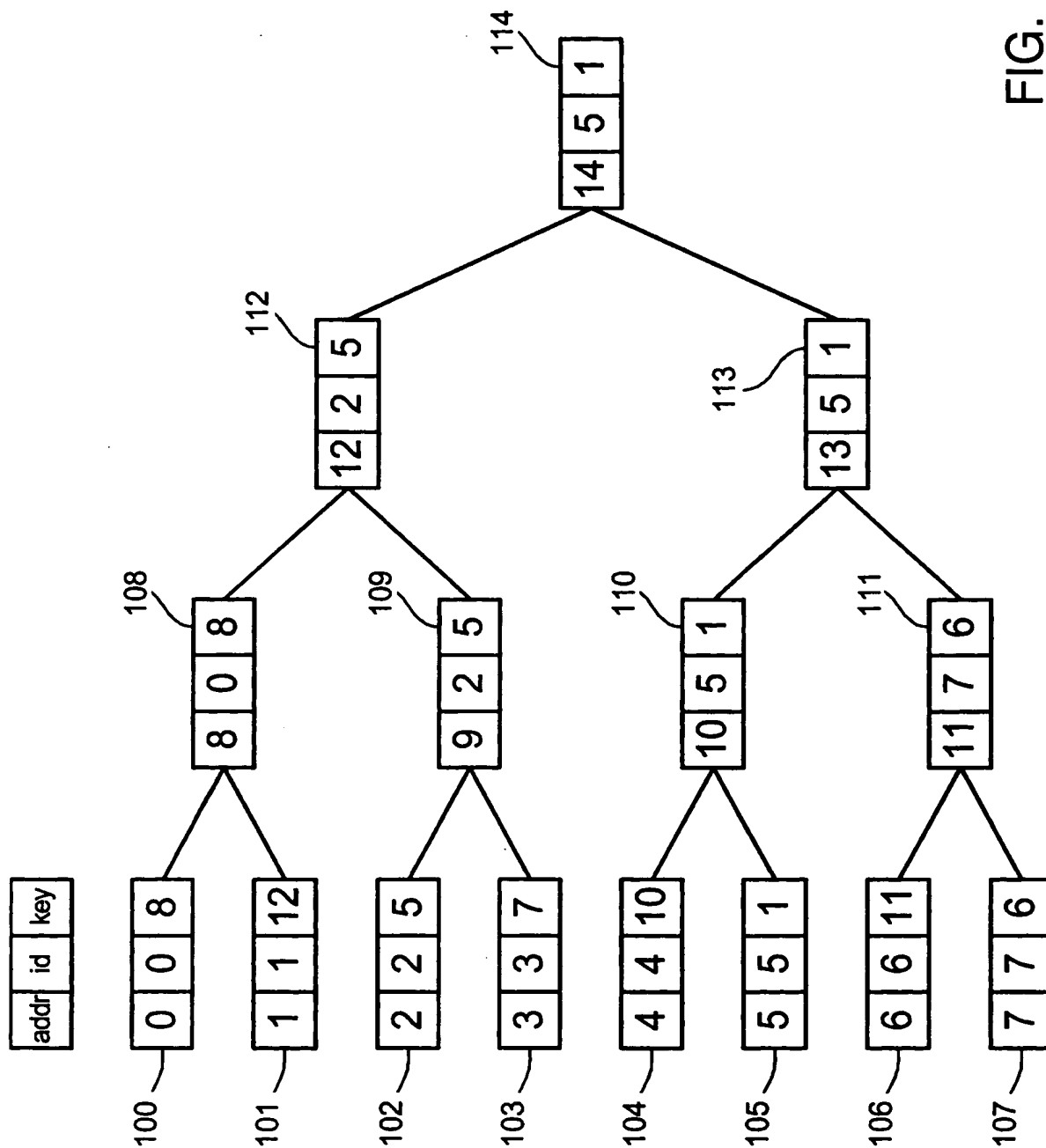
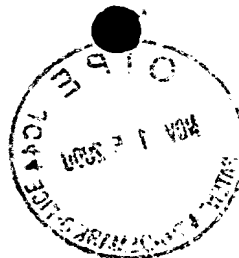


FIG. 1

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addr	id	key
------	----	-----

200

0	0	8
1	1	12
2	2	5
3	3	7
4	4	10
5	5	1
6	6	11
7	7	6
8	0	8
9	2	5
10	5	1
11	7	6
12	2	5
13	5	1
14	5	1

FIG. 2

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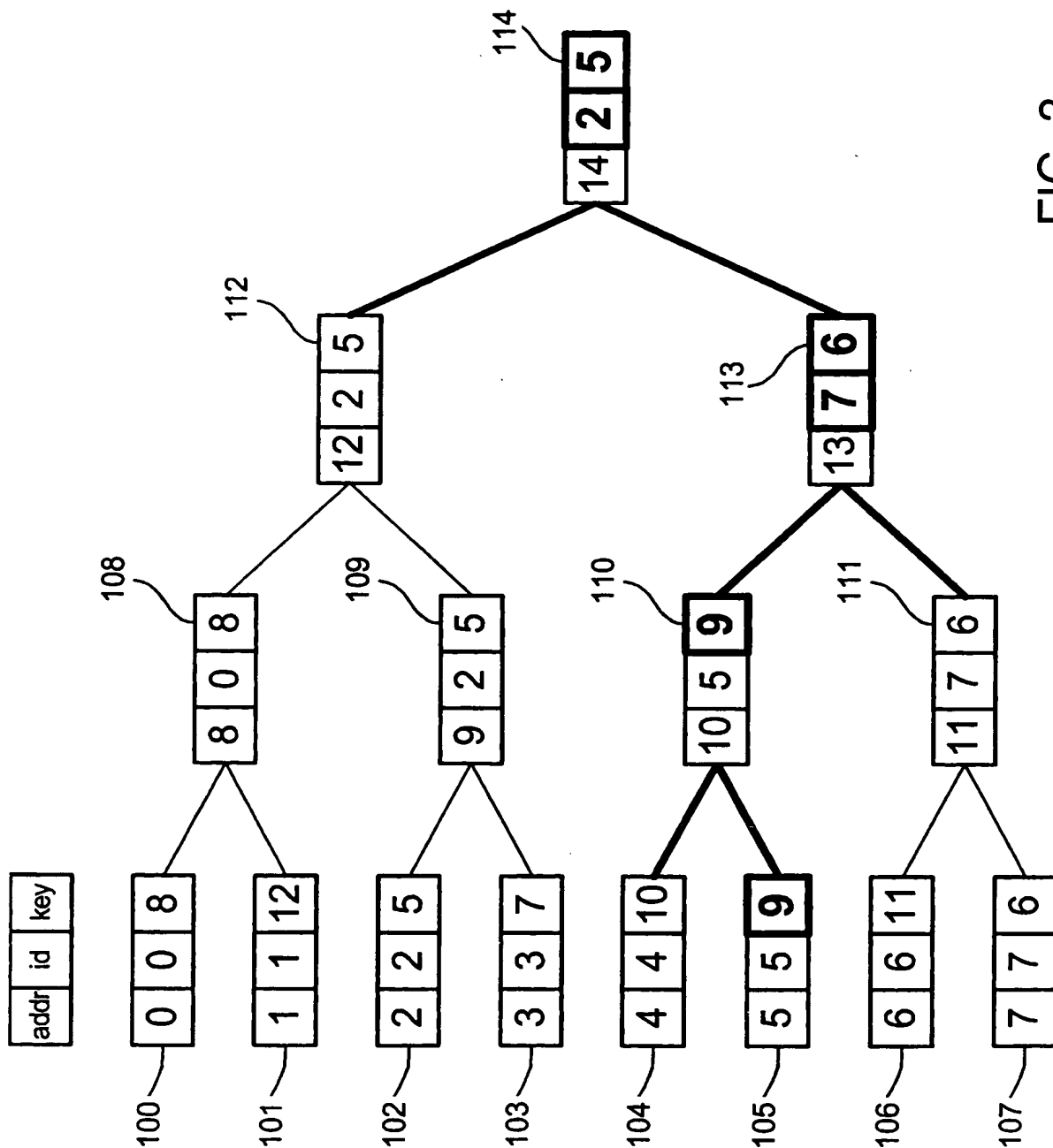


FIG. 3

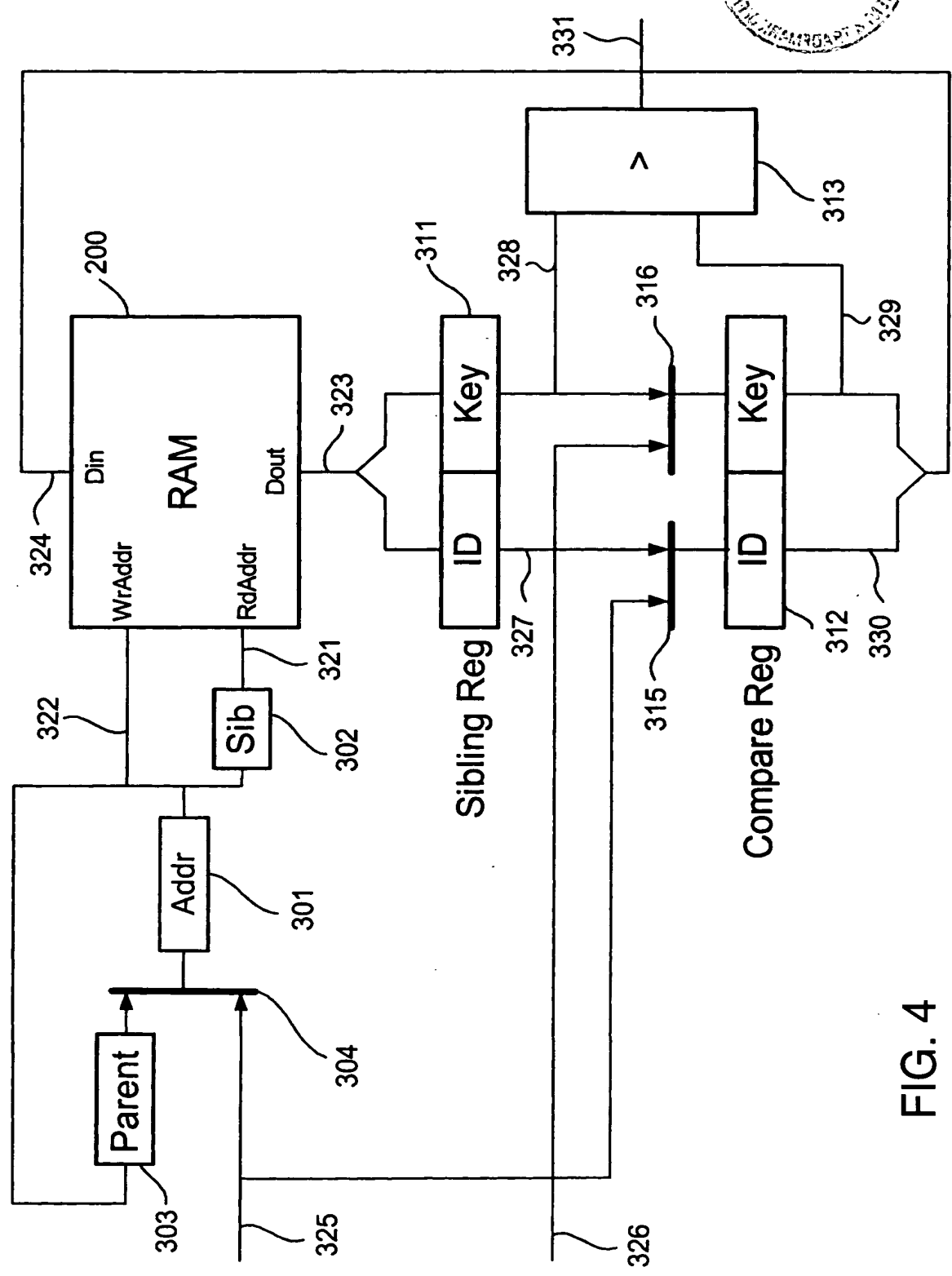


FIG. 4



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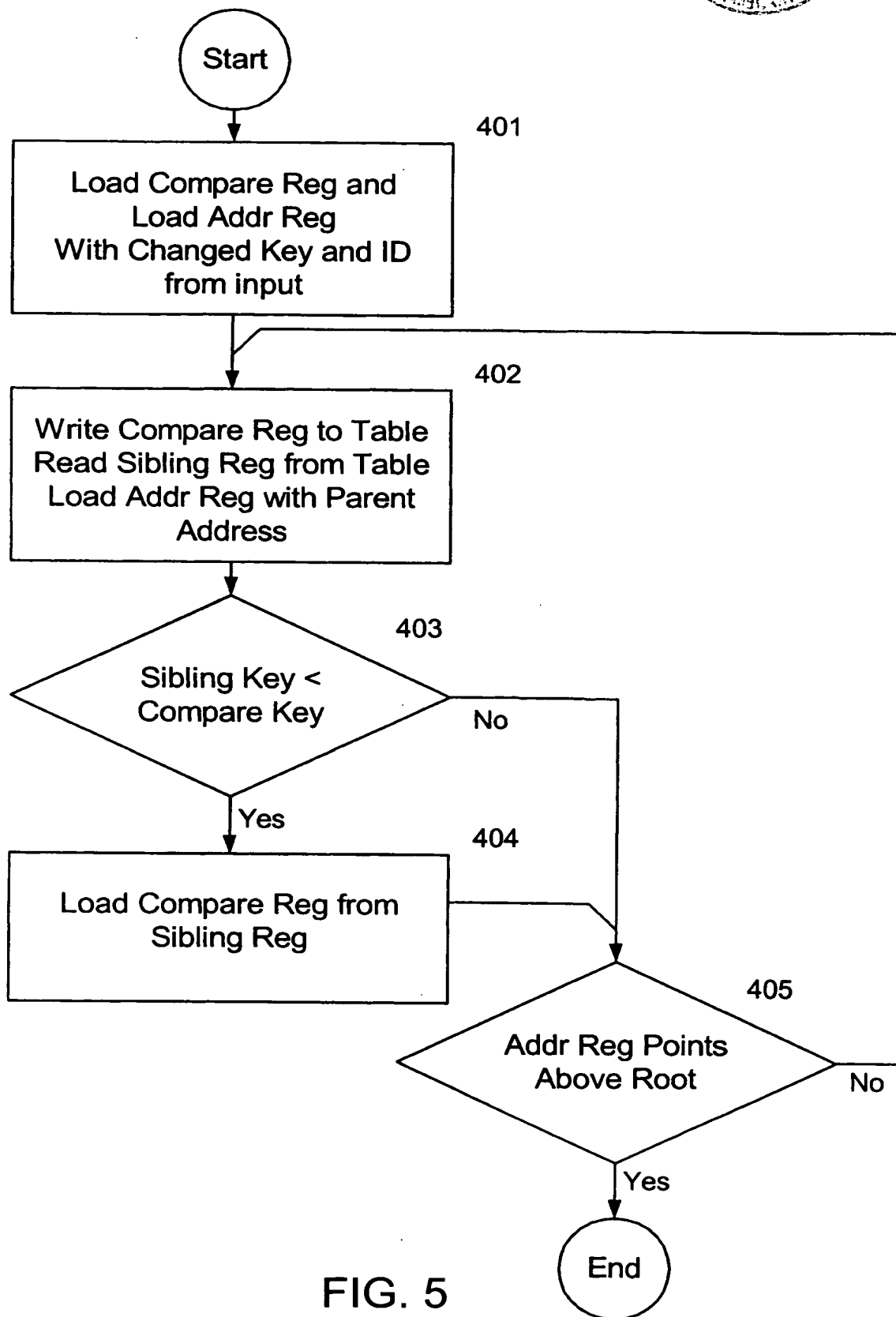


FIG. 5



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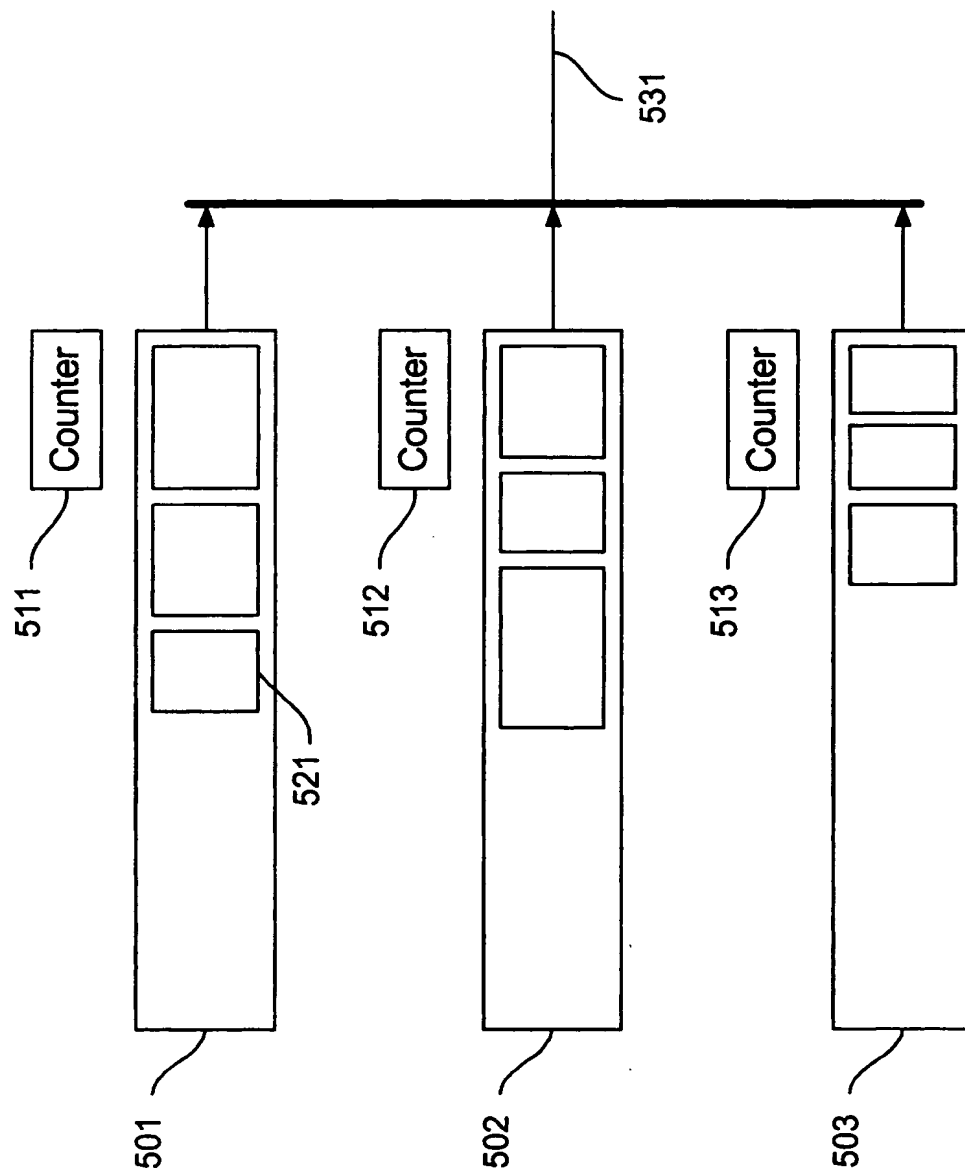


FIG. 6  
PRIOR ART

FIG. 8A
FIG. 8B
FIG. 8C

FIG. 8

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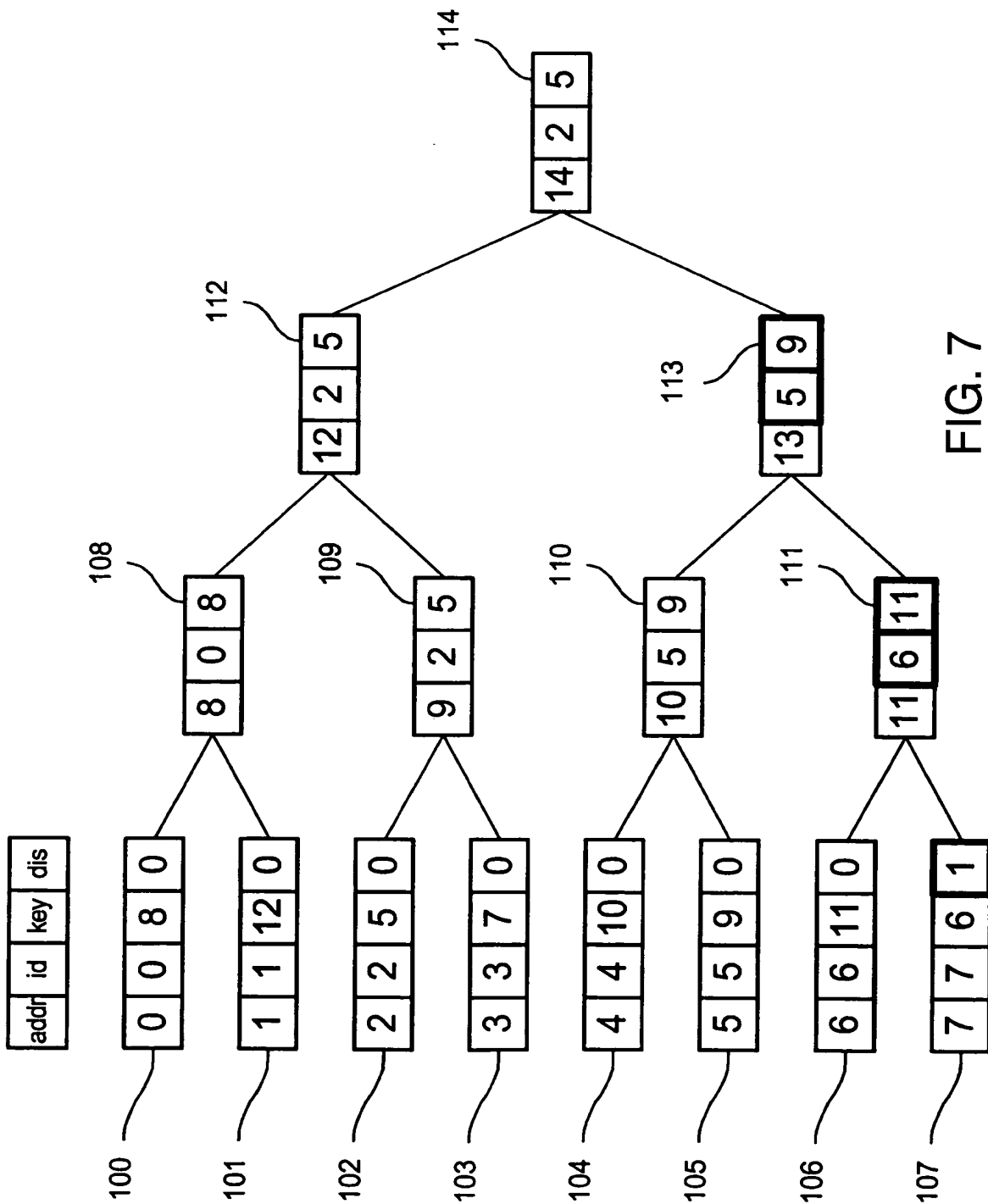


FIG. 7

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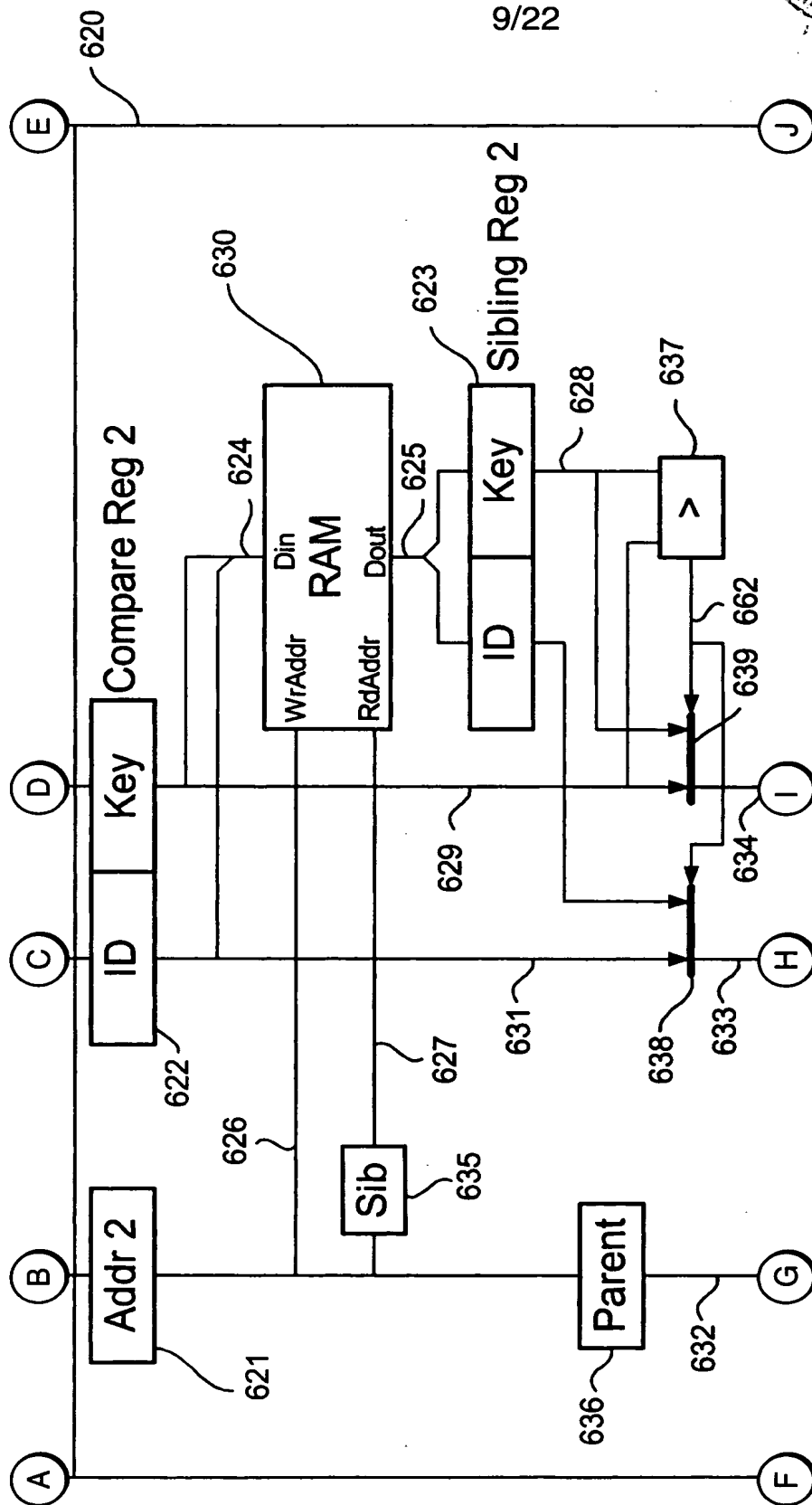


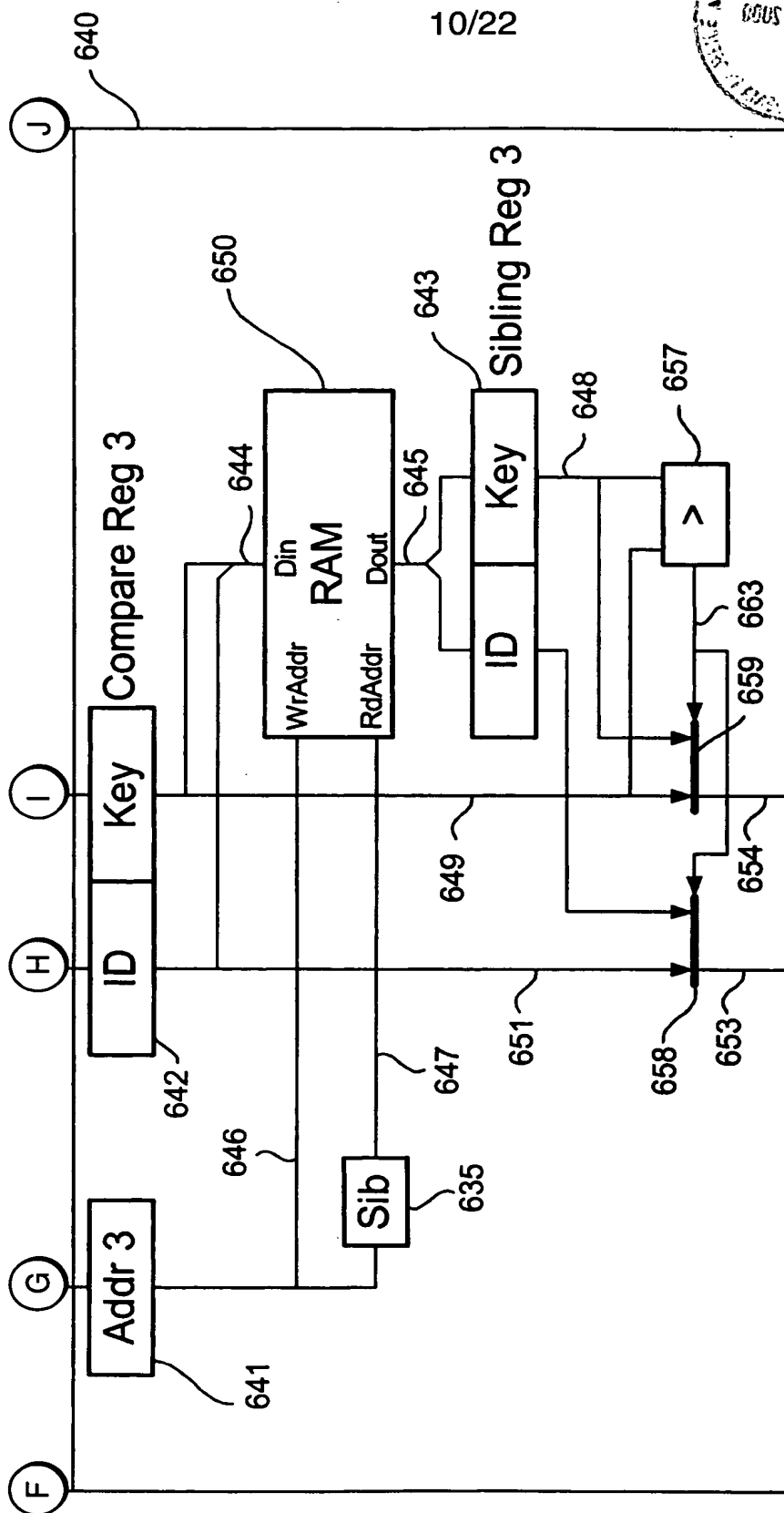
FIG. 8B

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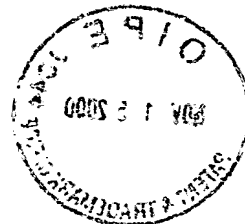


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	Cycle				
	1	2	3	4	5
Register					
Addr 1	5	7			
Comp 1	5.9	7.d	2.15		
Sib 1	4.10	6.11	3.7		
Addr 2		10	11	9	
Comp 2		5.9	6.11	3.7	
Sib 2		7.6	5.9	0.8	
Addr 3			13	13	12
Comp 3			7.6	5.9	3.7
Sib 3			2.5	2.5	5.9
Result			2.5	2.5	3.7

FIG. 9



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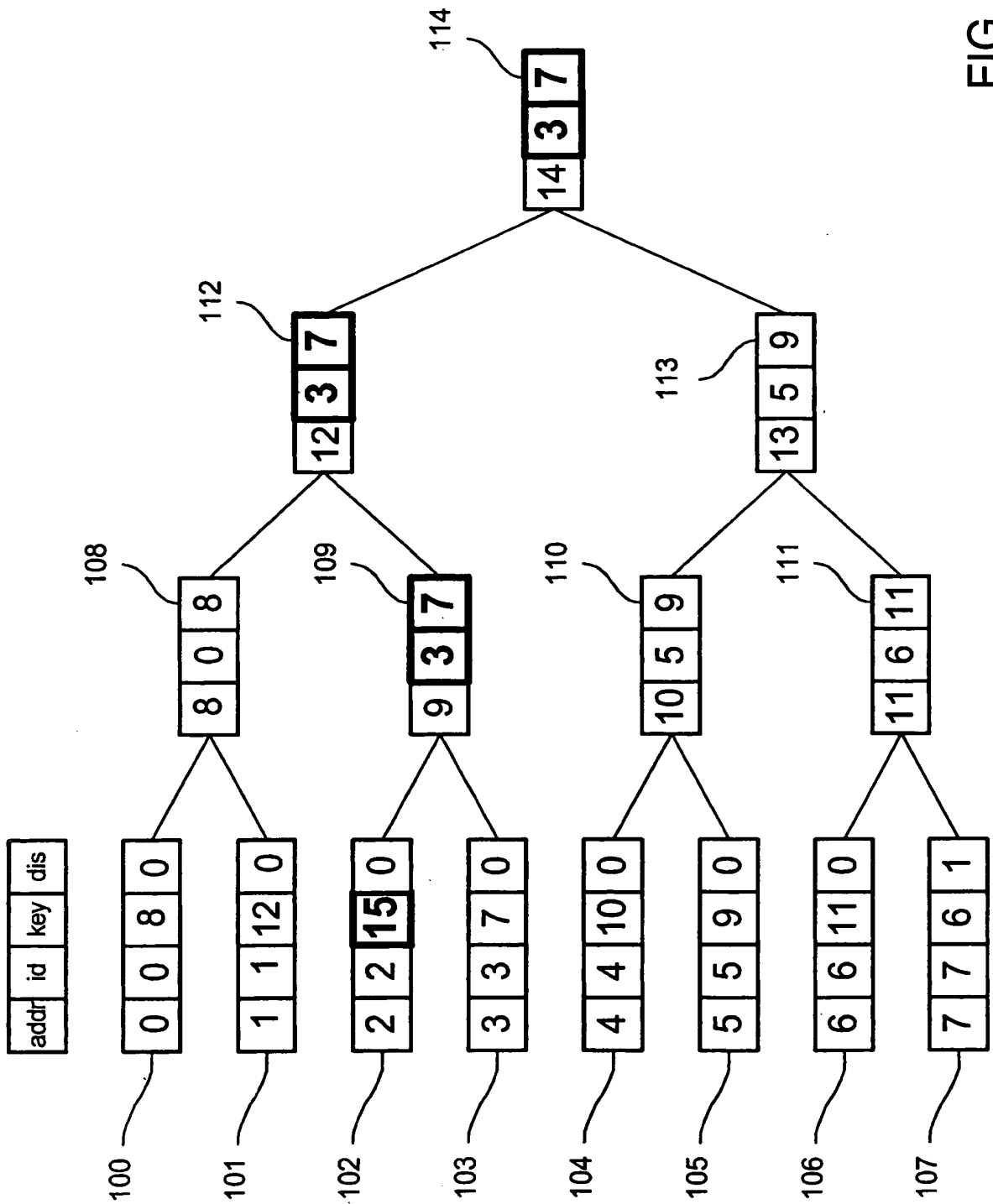


FIG. 10

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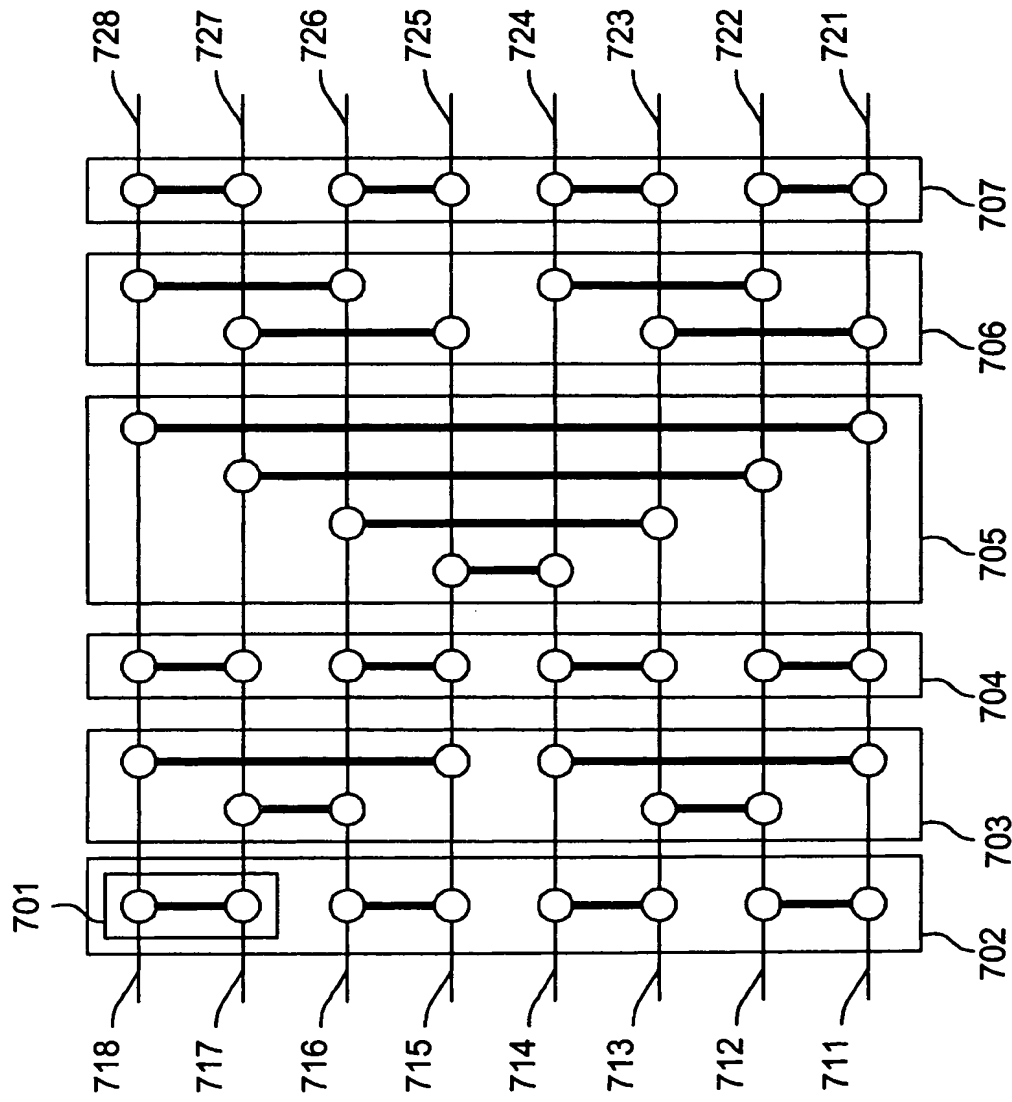


FIG. 11

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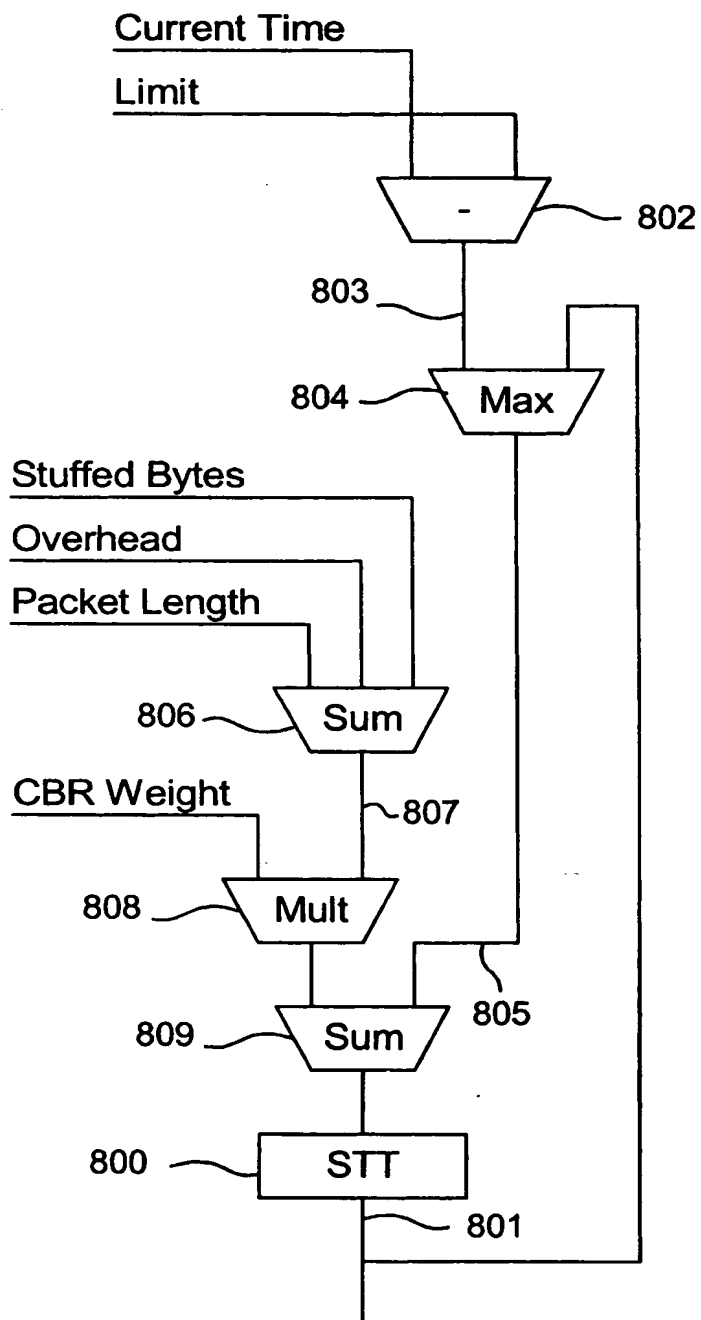


FIG. 12

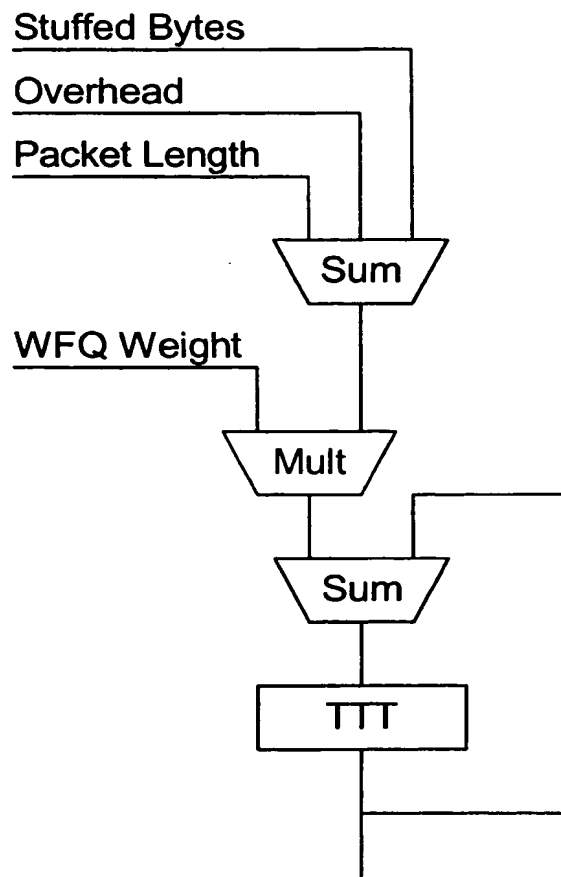
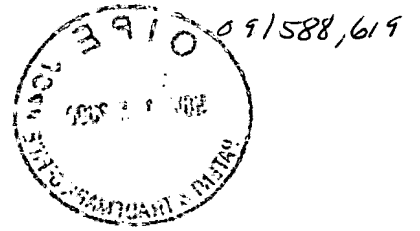


FIG. 13



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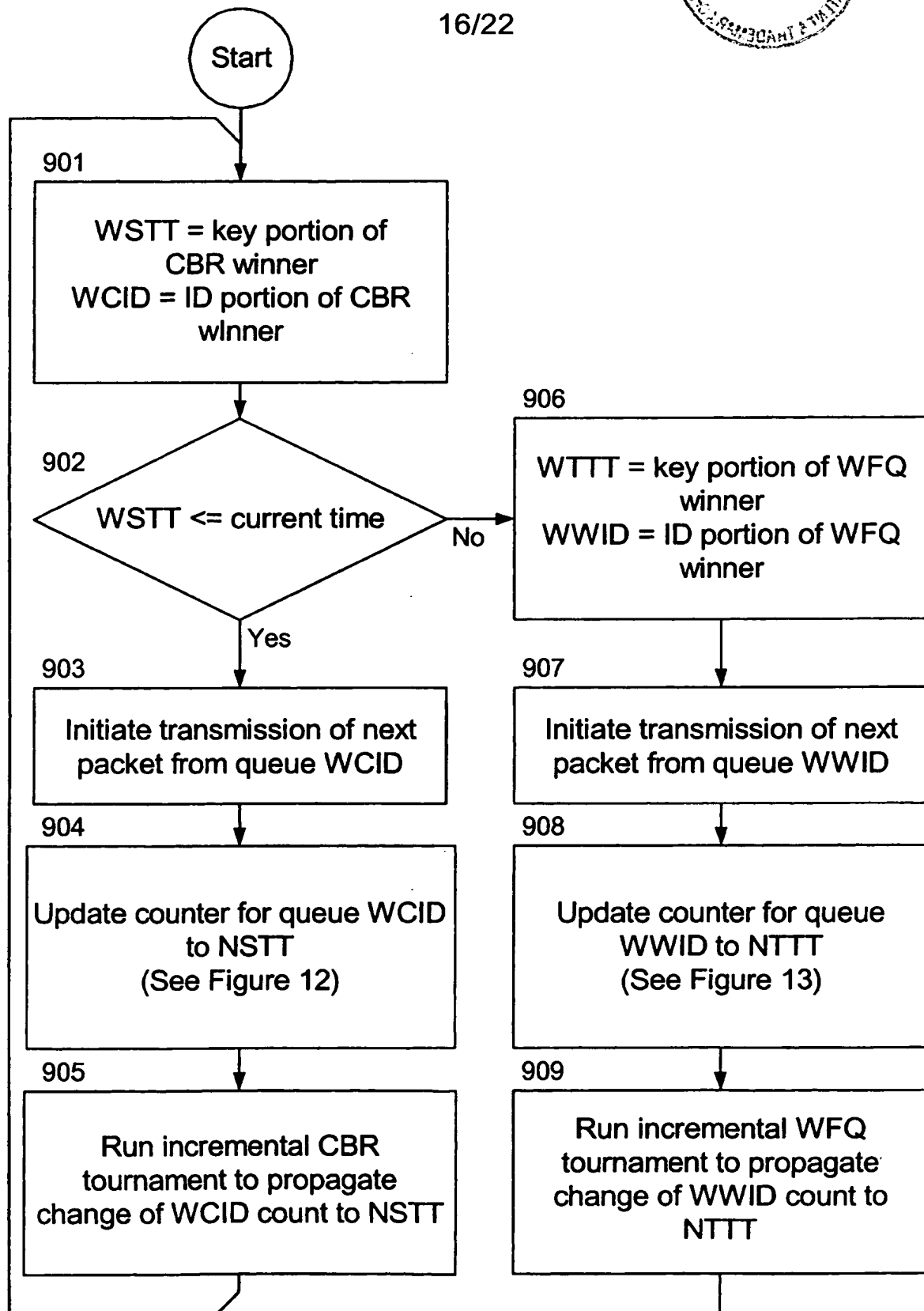


FIG. 14



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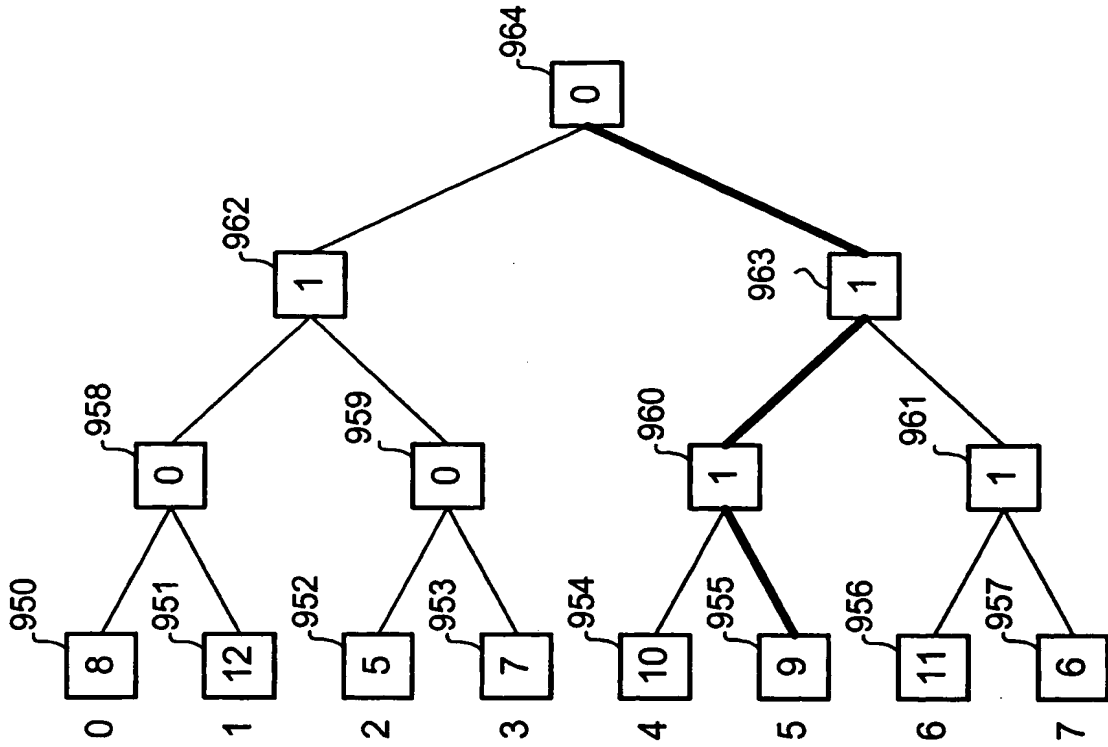


FIG. 16

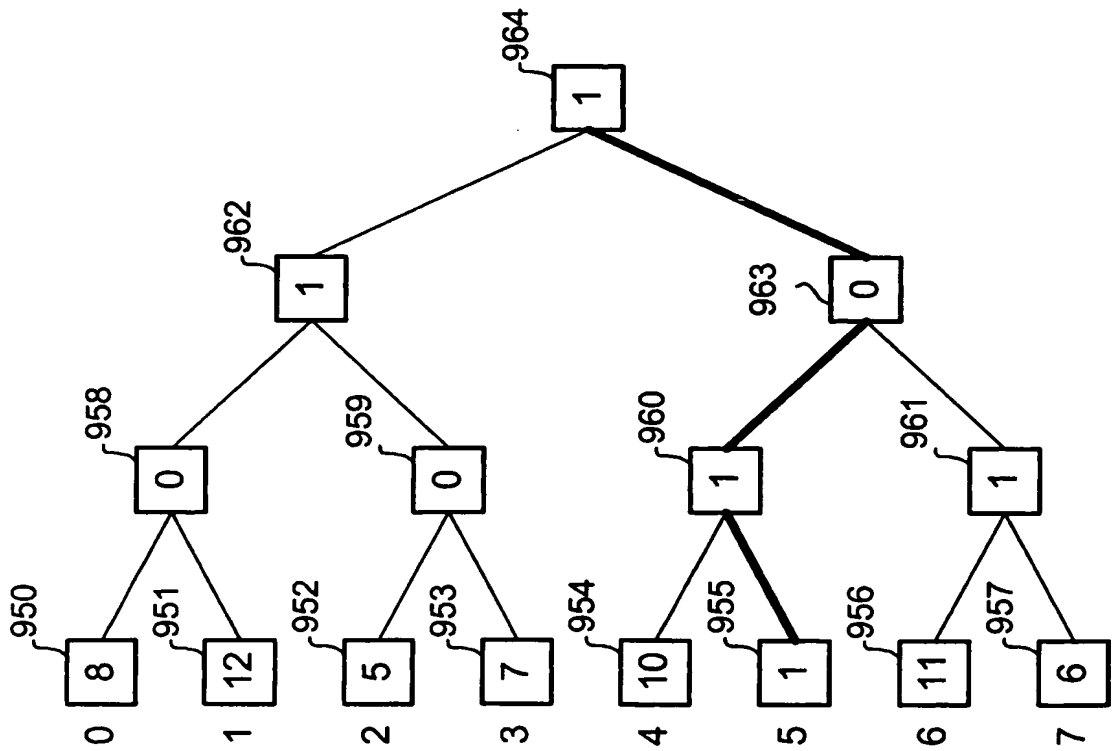


FIG. 15

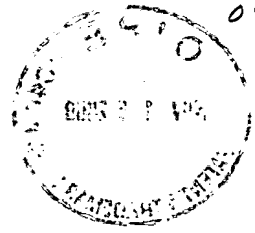
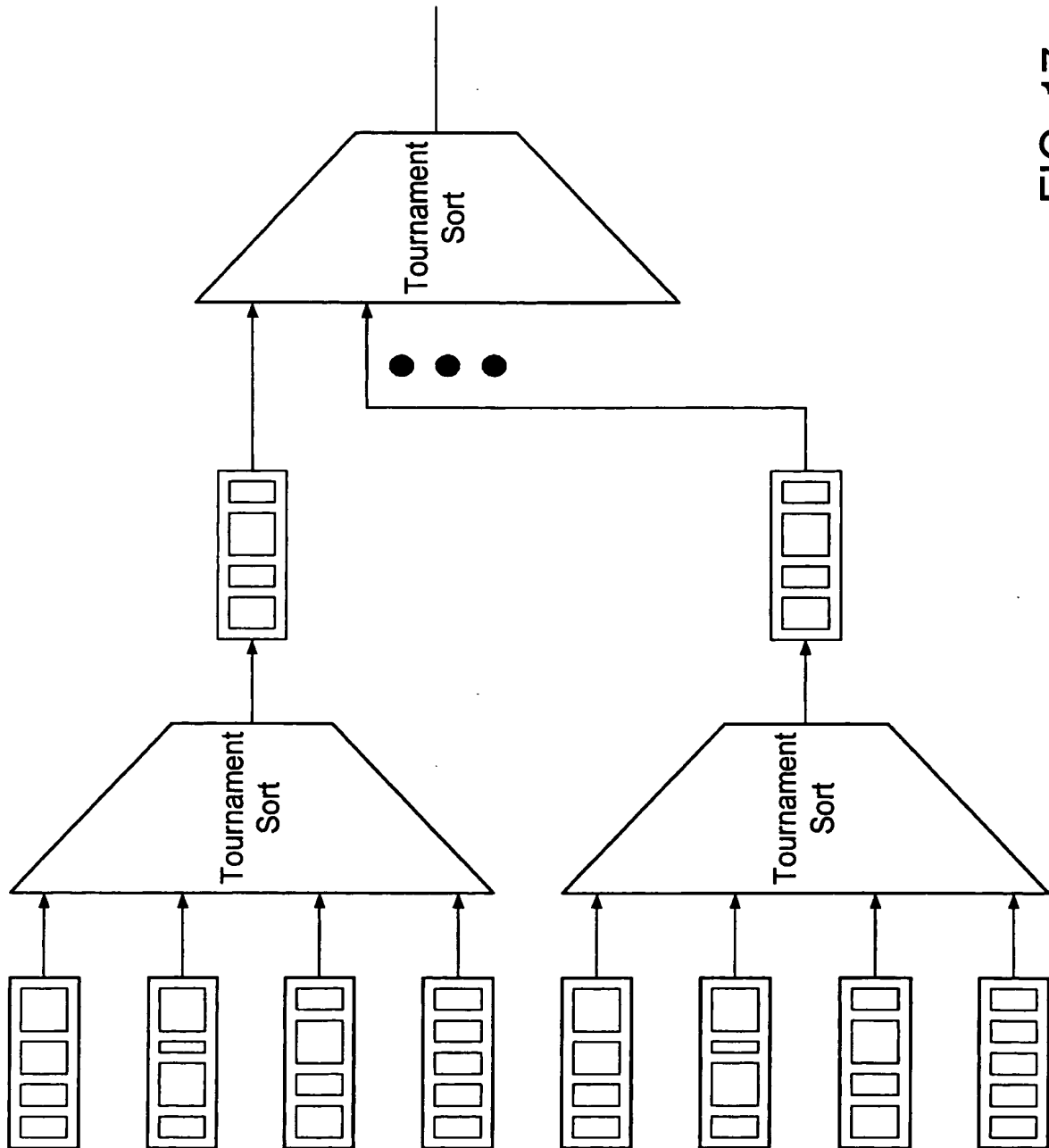


FIG. 17



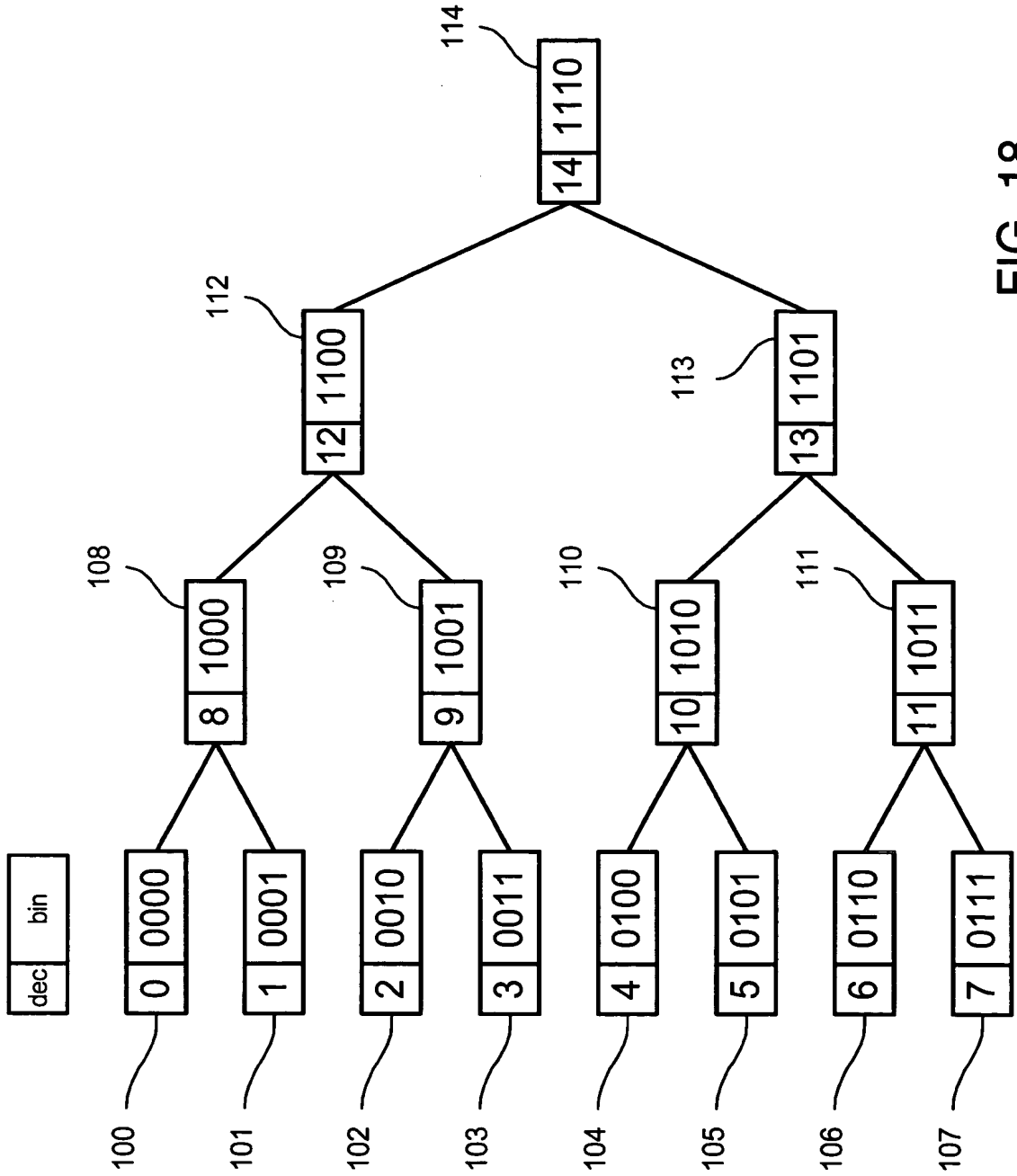


FIG. 18

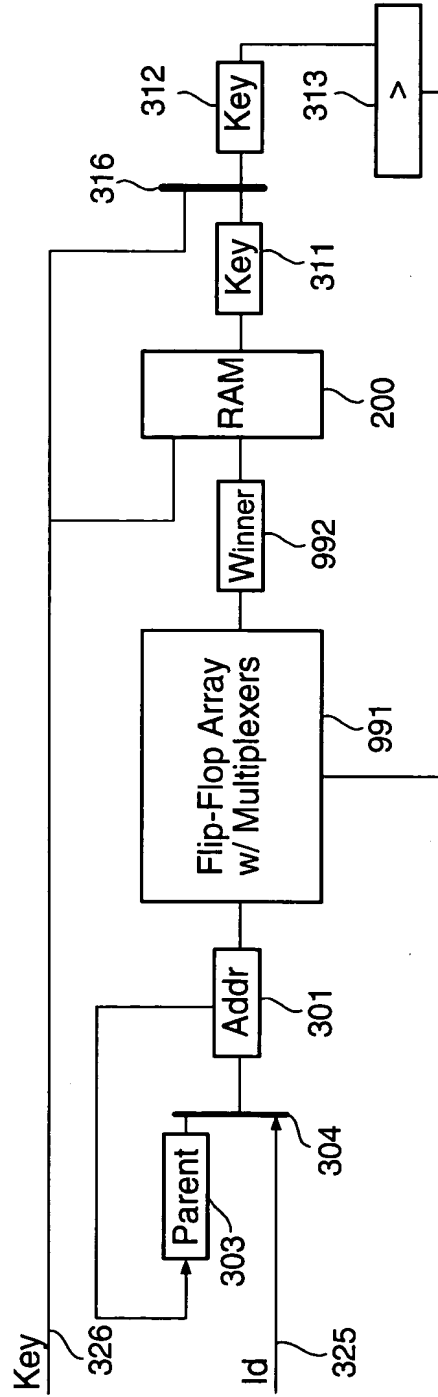


FIG. 19

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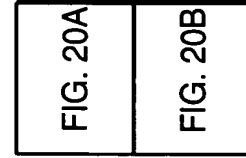


FIG. 20



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FIG. 20A

